# MODELING TRANSIENT THERMAL RESPONSE OF PULSED POWER ELECTRONIC PACKAGES

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*Abstract*

Steady-state power conversion applications have benefited from numerous packaging and cooling improvements, and there has been a push to apply the same techniques to pulsed power electronic systems and devices. However, the unique aspects of pulsed systems create a trade-off between high package thermal capacity for mitigating rapid temperature rise and low thermal resistance for rapid heat rejection. This report details a numerical study of several electronics packages with varying levels of cooling integration. Using Finite Element equivalent thermal circuit models to perform transient simulations of the packages, the effect of convective improvement and a reduced thermal path upon junction temperature response was examined.

Results showed that while a reduced thermal stack and high convection rate speeds the return to steady state after a pulse, the ability for improved convection to mitigate junction temperature rise diminishes significantly as pulse widths approach the thermal time constant of the package. In addition, the reduced thermal capacity of the integrated packages causes them to exhibit higher junction temperature rise and larger temperature swings than basic, non-integrated packages for certain pulse conditions. The worst case examined showed a direct die-cooling package exhibit a 3x increase in peak temperature and a 5x increase in pulse-to-pulse temperature swing over a standard, non-integrated package.

## I. INTRODUCTION

Efforts to improve the thermal performance of power conversion systems have led to the development of advanced cooling structures and packaging schemes for power electronic modules. Such improvements have involved enhancing convective performance [1], using high thermal conductivity materials [2], and reducing the number of layers in the package thermal stack [3]. These improvements have enabled significant decreases in thermal resistance between the cooling medium and the semiconductor devices which in turn allows for system operation at increased power and functional density. At the same time, numerous manufacturing and technology research communities have been increasingly investigating the use of pulsed power electronic systems for a variety of performance and capability improvements [4,5]. The specific definition of "pulsed" can vary greatly from one application to the next, but they generally feature repeated large, fast power draws at low duty cycles that can create a significant thermal design challenge. The large instantaneous heat loads must be managed for device protection and rejected quickly to support reasonable pulse rates, while at the same time meeting system size and weight goals associated with the cooling hardware. There has been a push to try to meet these goals by applying the same cooling improvement techniques to pulsed modules as have been proposed for systems operating in steady-state, or slowly varying conditions.

This report describes an analysis of typical improvements to steady-state power electronics packaging and their applicability to pulsed systems. Compact thermal models were used to quantify and compare the transient response of package designs with varying degrees of cooling integration. The impact of improved convection mechanisms and reduced packaging material upon power device temperature was quantified for varying pulse rates. It was hypothesized that the steady-state improvements might actually result in degraded pulsed thermal performance, and the simulations have shown this hypothesis to be correct under certain thermal conditions and package configurations.

### *A. Pulsed Electronics Thermal Behavior*

Concern arises with respect to applying the aforementioned package and cooling improvements to pulsed or transient power electronics systems because they were primarily intended to address the steady state portion of the package thermal impedance by minimizing overall thermal resistance ($R_{th}$) of the primary heat removal path. Pulsed power electronics systems typically have transient thermal load profiles with peak power draws significantly higher than the steady state average, a hypothetical example of which is shown in Figure 1. There are two distinct phases to the thermal conditions

# Report Documentation Page

*Form Approved*
*OMB No. 0704-0188*



| 1. REPORT DATE | 2. REPORT TYPE | 3. DATES COVERED |
|---|---|---|
| **JUN 2009** | **N/A** | **-** |

4. TITLE AND SUBTITLE
**Modeling Transient Thermal Response Of Pulsed Power Electronic Packages**

5a. CONTRACT NUMBER
5b. GRANT NUMBER
5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER
5e. TASK NUMBER
5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
**U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD 20783**

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
**Approved for public release, distribution unlimited**

13. SUPPLEMENTARY NOTES
**See also ADM002371. 2013 IEEE Pulsed Power Conference, Digest of Technical Papers 1976-2013, and Abstracts of the 2013 IEEE International Conference on Plasma Science. IEEE International Pulsed Power Conference (19th). Held in San Francisco, CA on 16-21 June 2013., The original document contains color images.**

14. ABSTRACT
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15. SUBJECT TERMS

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON |
|---|---|---|---|---|---|
| a. REPORT<br>**unclassified** | b. ABSTRACT<br>**unclassified** | c. THIS PAGE<br>**unclassified** | **SAR** | **6** | |

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resulting from the pulsed operation. First, the peak temperature rise is a function of the driving power pulse and the package thermal impedance. Second, the generally slower heat rejection phase during the 'off' portion of the duty cycle is entirely driven by the cooling mechanism, and in this period a 'thermal reset' must occur in time to prepare the system for the next pulse.

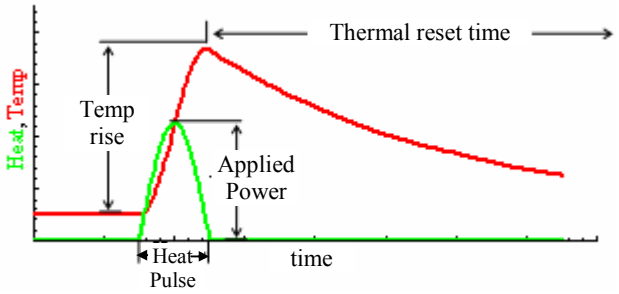


**Figure 1.** Representative low duty cycle pulsed thermal profile identifying the separate thermal factors.

Depending on the specific pulse rate and thermal profile, it should be noted that while the instantaneous power may impose an almost insurmountable cooling challenge, the average power over the full cycle may be much lower, possibly even by several orders of magnitude. Thus, designing a direct cooling system to manage the peak loads (if at all practical) could involve extensive overdesign relative to average power, especially in a low duty cycle system. Perhaps even more significant, however, as described by Meysenc [6] is that most of the previously described efforts to reduce package thermal resistance have also decreased local thermal capacitance ($C_{th}$). The thermal metrics $R_{th}$, $C_{th}$, and the thermal time constant, $\tau$, can be expressed using the following one-dimensional lumped element relationships:

$$R_{th} = x/kA_c \quad (1)$$

$$C_{th} = \rho c_p V = \rho c_p A_c x \quad (2)$$

$$\tau = R_{th} C_{th} = x^2 \rho c_p / k \quad (3)$$

where $A_c$ and $x$ are the layer cross-sectional area and thickness, respectively, and $k$, $\rho$, and $c_p$ are the material thermal conductivity, density and specific heat. As can be seen, decreasing package layer count and thickness decreases all three factors.

Meysenc's analysis showed that because a device's thermal capacity slows the related junction temperature rise, reducing package material (and capacitance) can make the devices more sensitive to a wider range of transient conditions. Whereas a package with higher time constant would damp out the thermal response above a certain frequency or pulse rate, packages with lower time constants would exhibit full temperature swings from higher frequencies such as are employed in pulsed systems. In addition, Cao and Krusius analyzed several heat absorption techniques and demonstrated that an optimized transient thermal solution must address both the need to absorb heat to reduce peak temperatures and the need for maximum heat removal to minimize the time to return to a steady state condition [7]. Doing both would achieve a minimum state of package overhead while meeting thermal requirements.

### *B. Thermal Circuit Modeling of Electronic Packages*

Equivalent circuit models of thermal systems are a convenient method of analyzing electronic packages. They can be derived from the linear lumped element solutions to heat conduction problem where temperature and heat flow are analogous to voltage and current, respectively [8]. Table 1 shows the equivalent electrical-thermal circuit elements. It can be surmised that the popularity of this method is due to the familiarity of circuit analysis to electrical designers, the ability to use available circuit simulation tools (e.g., SPICE simulators) to easily solve transient or steady state thermal systems, and the ability to solve coupled domain electrical-thermal models of electronic devices with that same simulation tool [9].

**Table 1**. 1D thermal equations and circuit equivalents

| Thermal Equation | Electrical Equivalent | Thermal Proportionality Constant | Standard Circuit Symbol |
|---|---|---|---|
| $q = \frac{kA}{l}\Delta T$ | $i = \frac{1}{R}\Delta v$ | $R_{th} = x/kA$ |  |
| $q = \rho c_p V \frac{dT}{dt}$ | $i = C\frac{dv}{dt}$ | $C_{th} = \rho c_p V$ |  |

Heat conduction problems can be modeled as networks of these thermal circuit elements using approximation techniques such as the Finite Difference Method (FDM) or the Finite Element Method (FEM). The solid body is discretized into individual nodes or elements with the conduction resistance and lumped thermal capacity assigned accordingly. Full details comparing both methods have been described by Ammous [10]. While each has its particular strengths and weaknesses, Ammous showed that FEM's thermal capacity representation at boundary nodes can enable improved accuracy at those nodes with similar discretization levels for large, fast transients. Thus, the FEM representation is used in this study as such high rate transients are expected to occur.

Figure 2 shows both a single element equivalent circuit and element chain representing a discretized solid body as derived by Hsu and Vu-Quoc [11]. The current source on the left side represents a heat source into the system, and the voltage source on the left side represents a fixed temperature boundary condition. Determining the values for $R_{th}$ takes the form shown in (1), but slightly different forms of capacitance are used to represent the distinction between nodal and mutual capacitance terms in the Finite Element Formulation. These are given by:

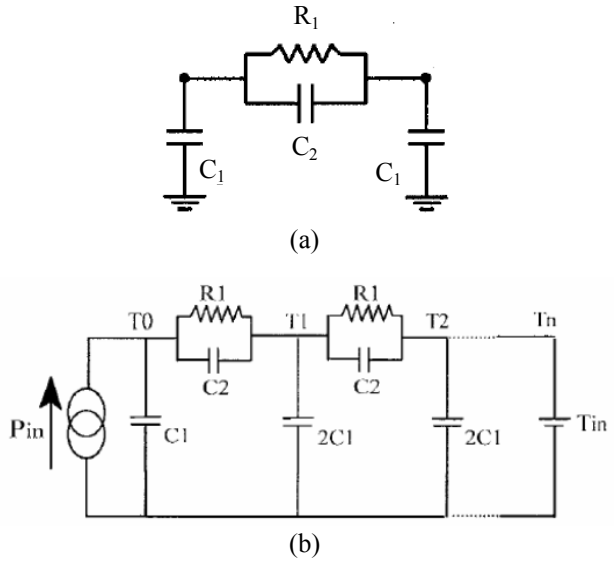


**Figure 2.** Finite Element equivalent thermal circuit representations. (a) Single element. (b) Element chain representing a discretized body. From [11].

$$C_1 = \frac{1}{2}C_{th} = \frac{1}{2}\rho c_p A_c x \qquad (4)$$

$$C_2 = \frac{1}{6}C_{th} = \frac{1}{6}\rho c_p A_c x \qquad (5)$$

Also, for shared nodes, the capacitance to ground will be the sum of the two element nodal $C_1$ values (shown as $2C_1$ in Figure 2(b) because both elements have the same $C_1$).

## II. MODELING APPROACH

### *A. Electronic Package Thermal Stacks*

Five power electronic package stacks are examined in this study to compare the transient impact of improvements typically proposed for steady-state thermal applications. The five packages, referred to hereafter as Cases 1-5, are shown in Figure 3. Case 1 is the basic high-power electronics package consisting of a semiconductor device mounted on an AlN DBC board and a copper baseplate which is affixed to an aluminum heat sink or cold plate using a thermal interface material (TIM). In Case 2, the package resistance is reduced by rigidly affixing the heat sink or cold plate to the copper baseplate. In Case 3, the convective mechanism is integrated into the baseplate and directly cools the back of the DBC substrate. In Case 4, the cooling is integrated directly into the ceramic substrate. Finally, in Case 5, the coolant is applied directly to the backside of the device. Package material parameters used for simulation are listed in Table 2.

**Table 2.** Package material thermal properties

| | $k$ [W/mK] | $\rho$ [kg/m$^3$] | $c_p$ [J/kgK] |
|---|---|---|---|
| Si | 135 | 2330 | 704 |
| Cu | 400 | 8933 | 385 |
| AlN | 180 | 3330 | 736 |
| Al | 200 | 2700 | 880 |
| AuSn | 57 | 19720 | 129 |
| T.I.M. | 4 | 3230 | 1100 |

Using (1), (2), and (3) and the layer thicknesses, the resistive and capacitive components of each layer can be calculated along with the associated thermal time constant for a unit device area. These thicknesses and associated values are shown in Table 3. It should be noted that each Case uses the same device layer thicknesses except for Case 4, where it is assumed that about a half-thickness of AlN (300 µm) remains through which heat must conduct. Also, the device junction is called out as a discrete layer (with the same silicon properties) to permit improved boundary condition fidelity. Table 4 gives the accumulated thermal resistivity, capacity, and time constant for each package. From that data it can be seen that while the cooling integration is having the desired effect of significantly reducing thermal resistivity, they also significantly reduce package thermal capacity and thermal time constant.

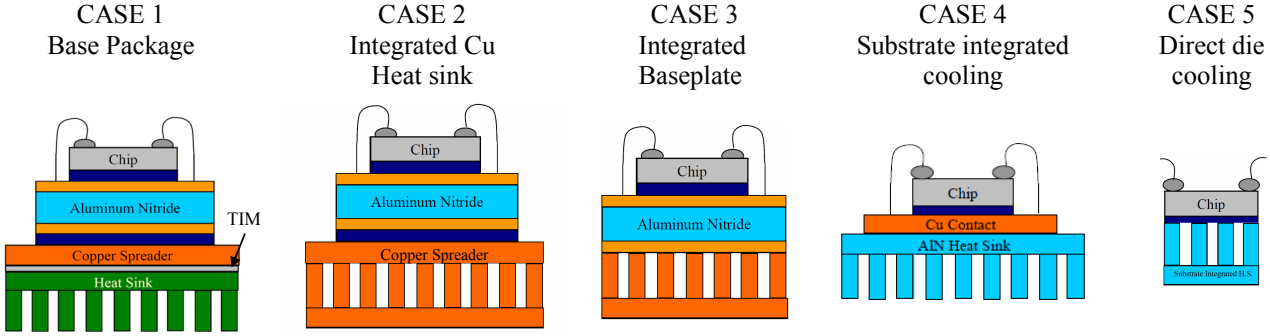


**Figure 3.** Package configurations examined as a part of this study. Cases 2 through 5 represent increasing levels of cooling integration into the package thermal stack.

**Table 3**. Package layer thermal characteristics

| layer | *x*[mm] | R" [cm$^2$K/W] | C" [J/cm$^2$K] | RC [ms] |
|---|---|---|---|---|
| junction | 0.100 | 0.007 | 0.016 | 0.122 |
| die | 0.400 | 0.030 | 0.066 | 1.94 |
| die attach | 0.050 | 0.009 | 0.013 | 0.112 |
| DBC, Cu | 0.300 | 0.008 | 0.103 | 0.774 |
| DBC, AlN | 0.625 | 0.035 | 0.153 | 5.32 |
| DBC, Cu | 0.300 | 0.008 | 0.103 | 0.774 |
| sub. attach | 0.100 | 0.018 | 0.025 | 0.446 |
| baseplate | 3 | 0.075 | 1.032 | 77.4 |
| T.I.M. | 0.050 | 0.125 | 0.018 | 2.22 |
| Al Sink | 5 | 0.250 | 1.188 | 297.0 |

**Table 4**. Total thermal characteristics for each Case

| Case | R" [cm$^2$K/W] | C" [J/cm$^2$K] | Σ RC [ms] |
|---|---|---|---|
| 1 | 0.563 | 2.717 | 386.1 |
| 2 | 0.188 | 1.511 | 86.87 |
| 3 | 0.096 | 0.454 | 9.044 |
| 4 | 0.070 | 0.271 | 4.176 |
| 5 | 0.037 | 0.082 | 2.066 |

### *B. Convection Approximation*

We adopted an *equivalent flat plate convection* technique as used by O'Keefe in a study of steady state power package behavior [12]. In this technique, an effective convection coefficient, $h_{eff}$, is defined for each cooling mechanism as:

$$h_{eff} = h \cdot AR \cdot \eta \tag{6}$$

where $h$ is the cooling mechanism's average convection coefficient over the wetted surfaces, $AR$ is the area enhancement ratio of wetted surface area to cross-sectional area, and $\eta$ is an area utilization efficiency term (comparable to heat sink fin efficiency.) More details as to determining $h_{eff}$ for specific cooling methods can be found in the aforementioned study by O'Keefe. In this study $h_{eff}$ is allowed to vary from 200 to 500,000 W/m$^2$K, representing the range from forced air cooling on a heat sink to some of the higher reported rates for single phase forced liquid cooling [13]. A convective cooling mechanism is represented in the thermal circuit by a thermal resistor connected to ground, where the value of that resistor is derived from:

$$q_{conv} = h_{eff} \cdot A_c \left(T_s - T_f\right) \tag{7}$$

$$R_{th,conv} = \Delta T / q_{conv} = 1 / h_{eff} \cdot A_c \tag{8}$$

$T_s$ and $T_f$ are the convective surface and fluid temperatures, respectively.

### *C. Simulation Procedure*

The circuits in this study were simulated using the freely available SPICE simulator LTspice IV by Linear Technology Corporation [14]. The FEM thermal circuit model for Case 1 is shown in Figure 4. Cases 2-5 are modeled similarly, with fewer elements according to each Case's configuration. Unit step response simulations were run while sweeping the convection coefficient over the range of 200 - 500,000 W/m$^2$K to determine steady-state package behavior. Next, a single unit square pulse was applied to each Case, sweeping both convection coefficient and pulse width (from 50µs - 10sec), to quantify the ability of improved convection to reduce peak junction temperature. A frequency domain small signal analysis was then run for each case and convective rate to examine the claims made by Meysenc regarding package inertia. Finally, transient analyses were run with unit power pulse trains to examine the same behavior in the time domain. A unit power was used throughout the study under the assumption that results will be linear and the resultant thermal impedance values will be representative over a wide range of power levels.

## III. RESULTS AND DISCUSSION

### *A. Steady-State Behavior*

Figure 5 shows the steady-state package responses as extracted from the unit step junction profiles. Flux normalized temperature rise and thermal time constants showed high dependence on convective rate, as expected. Both $R_{th}$ and $RC$ trend toward the package values that were shown in Table 4. It is assumed that the Case 5 discrepancy is due to inadequacy of the lumped element approximation for very low impedance packages.

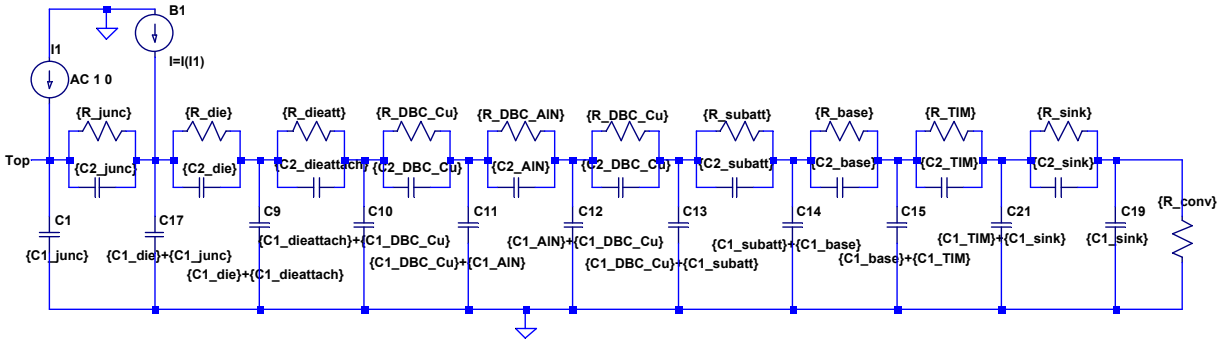


**Figure 4.** CASE 1 SPICE thermal circuit representation with each package layer represented as a single element.

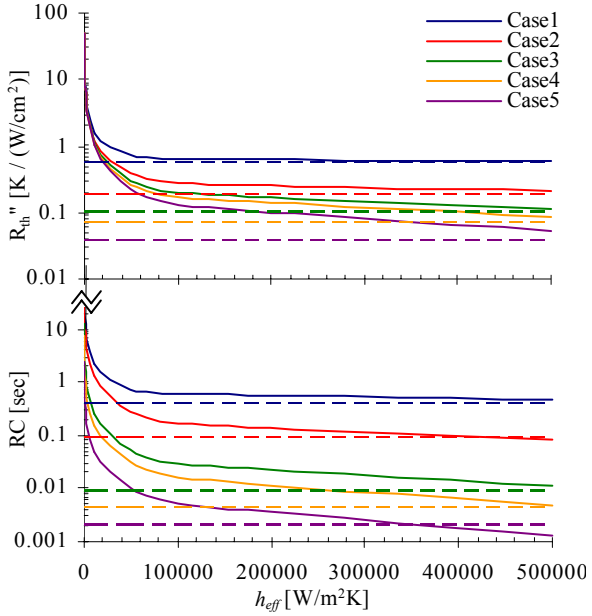


**Figure 5.** Steady state $R_{th}$ and $RC$ time constant of the modeled packages. The dashed lines represent the limiting values as $h_{eff}$ approaches infinity.

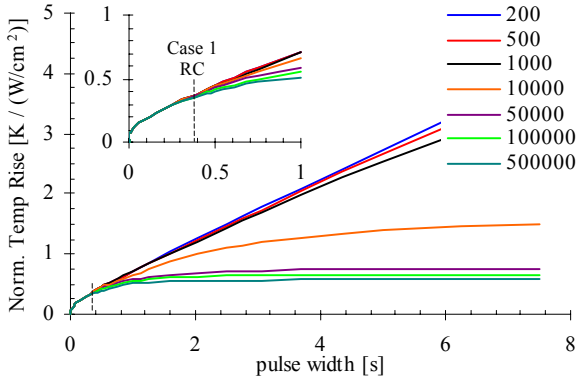


**Figure 6.** Case 1 junction temperature rise as a function of convection rate and pulse width.

### *B. Improved Convection on Pulsed Temperature Rise*

The Case 1 results from simulating a unit pulse applied to the package with varying convection and pulse width are shown in Figure 6. As expected, for long pulse-widths the peak temperature rise is highly dependent on the convective resistance. However, as the pulse widths decrease the device junction becomes thermally decoupled from the heat sink. As shown in the Figure 6 inset, despite a three orders-of-magnitude change in convection the variation in junction temperature rise is negligible for pulses below the package RC constant.

### *C. Frequency-Domain Junction Response*

The AC response of the different packages for three different convection rates are shown in. Figure 7. From these graphs it can be seen that the behavior described by Meysenc indeed does occur for integrated power electronic packages. For all three convection rates shown,

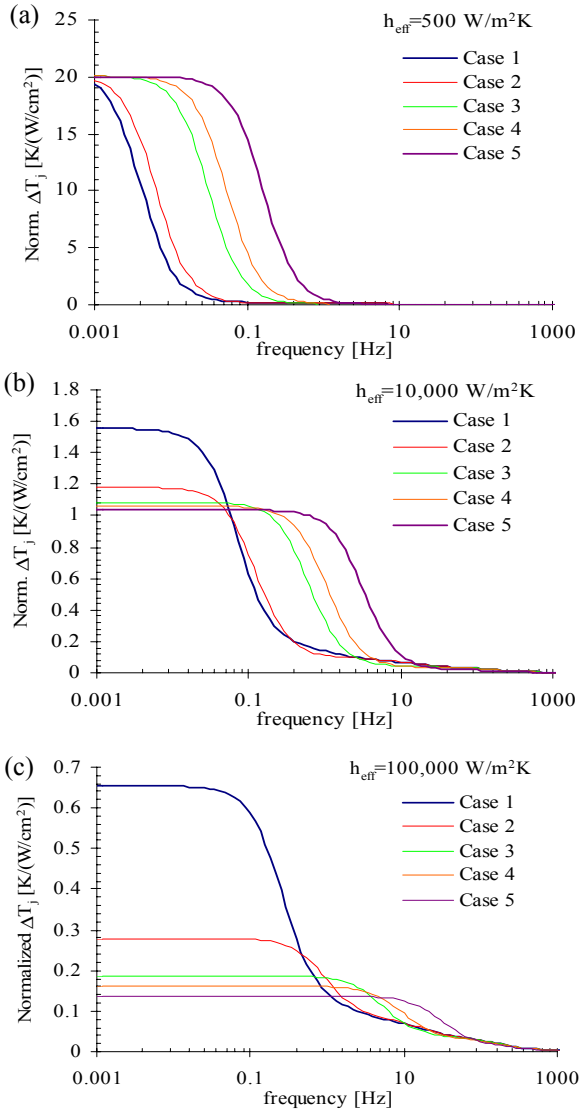


**Figure 7.** frequency domain response of the packages for three different convection conditions.

a switching frequency range exists where the improved packages have worse peak junction temperature performance than even the base Case 1 package. As expected increased convection does begin to diminish the magnitude of this effect, and it also shifts the aforementioned frequency range to higher frequencies

### *D. Time-Domain Junction Response*

Figure 8 shows the junction temperature response of Cases 1, 3 and 5 (with $h_{eff}$ = 10,000 W/m$^2$K) to a square pulse train with unit power, 1 second period, and 10% duty cycle equating to a 100 ms pulse width. The last set of pulses in the pulse train is shown in the graph (well after the slower Case 1 package has achieved steady-state temperature oscillations). It is clear from the temperature profiles that the "improved" packages 3 and 5 are actually performing worse with respect to peak temperature rise. The minimum and maximum temperatures seen by the

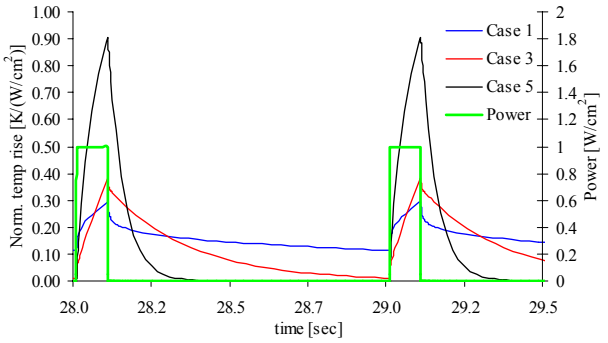


**Figure 8.** Junction temperature rise for Cases 1, 3 and 5 during a unit square pulse train with 1-second period, 10% duty cycle, and $h_{eff}$ = 10,000W/m$^2$K.

junction during the pulses are listed in Table 5. The faster thermal responses of Cases 3 and 5 cause peak temperatures to exceed Case 1 by 30% and 207%, while the increased heat rejection rates leads to temperature swings 106% and 401% larger, also. This case shows that although the absolute magnitudes of the AC analysis may not directly translate to pulsed response, the qualitative result of degraded performance over certain operating regimes appears to be valid. As expected, however, the integrated packages do thermally reset much faster than the base package. This would permit devices to switch at higher pulse rates without resulting temperature increases. Obviously, application specifics will need to dictate which conditions are preferred.

**Table 5.** Normalized temperature rise for Cases 1, 3, 5

| Case | $T_{min}$ [K/(W/cm$^2$)] | $T_{max}$ [K/(W/cm$^2$)] | $T_{max}$ % diff | $\Delta T$ [K/(W/cm$^2$)] | $\Delta T$ % diff |
|---|---|---|---|---|---|
| #1 | 0.11 | 0.29 | -- | 0.18 | -- |
| #3 | 0.01 | 0.38 | 30 | 0.37 | 106 |
| #5 | 0 | 0.90 | 207 | 0.90 | 401 |

## IV. CONCLUSIONS

In this study we examined a series of power semiconductor package configurations to determine their effectiveness for pulsed applications. Using thermal equivalent circuit models, we examined whether thermal stack improvements designed for steady-state applications would be beneficial under pulsed loads. We were able to demonstrate two key points. First, while convection is effective in driving the return to the steady-state condition and enabling high pulse rates, there are diminishing returns (to the point of becoming negligible) in its ability to reduce peak junction temperatures as pulse widths approach the time constant of the thermal package. Second, the decreasing thermal capacity that occurs with further integration of the cooling mechanism into the package does create the potential for increased peak temperatures and increased magnitude in temperature swing. Thus, pulsed electronics designers cannot blindly borrow solutions from steady-state systems and expect to see similar performance improvements. Successful development of electronic packages for pulsed applications will demand a thorough analysis of the tradeoff between thermal resistance and capacitance with respect to the specific requirements and limitations of the task at hand.

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